Atty. Docket No. OPP-GZ-2004-0020-US-00
Serial No: 11/026,643

Remarks

Claims 1-7, 9-14 and 17-23 are active in this application.

Applicant and his representatives wish to thank Examiner Nguyen for the thorough examination of the present application, the detailed explanations in the Office Action dated December 15, 2005, and the professional and courteous discussion held with their undersigned representative on February 7, 2006. Claim 1 has been amended as discussed. Support for the amendments can be found in paragraphs [0032]-[0034], for example. Also, a Rule 132 Declaration is submitted herewith to explain the results provided by the claimed invention. No new matter is introduced by the present Amendment.

The present invention relates methods for fabricating a semiconductor device. In one aspect, the present invention relates to a semiconductor device comprising:

a) cleaning a semiconductor substrate with a transistor formed thereon, the transistor including a source electrode, a drain electrode and a gate electrode;

b) placing the cleaned semiconductor substrate into a sputter chamber in a deposition equipment, and heating the semiconductor substrate to a temperature of from greater than 450 to 600°C;

c) initially forming a monosilicide at the same time as depositing a metal film under a state where the semiconductor substrate is heated at the temperature of from greater than 450 to 600°C;

d) removing residual metal film not used for the formation of silicide; and

e) annealing the semiconductor substrate (see amended Claim 1 above).

In a second aspect, the method comprises:

1) cleaning a semiconductor substrate with a transistor thereon, the transistor including a source electrode, a drain electrode and a gate electrode;

2) placing the cleaned semiconductor substrate into a sputter chamber and sputtering a metal film at a DC power of 2 – 10kW, while heating the semiconductor substrate at a temperature of 450 to 600°C to form silicide;
3) removing residual metal film; and
4) annealing the semiconductor substrate (see Claim 17 above).

As discussed in the attached Declaration of Jae-Won Han, experiments were performed to determine the processing time savings provided by the present invention, as compared to a conventional process reasonably close to the present invention, to support patentability of claim 1 as set forth above. Also, experiments were performed to demonstrate the commercial importance of the results provided by the embodiment of the invention recited in claim 17. Thus, the present claims are patentable over the cited references.

The Rejection of Claims 1, 2, 9, 12-14, 17, 18 and 21-23 under 35 U.S.C. § 103(a)

The rejection of Claims 1, 2, 9, 12-14, 17, 18 and 21-23 under 35 U.S.C. § 103(a) as being unpatentable over Hamanaka (U.S. Pat. No. 6,337,272) is respectfully traversed.

Hamanaka relates to a method of manufacturing silicide, including the steps of forming a transistor on a substrate (see, e.g., Hamanaka, col. 11, ll. 57-61), removing a native oxide film from the surface of the substrate (see, e.g., Hamanaka, col. 12, ll. 7-10), placing the semiconductor substrate in a sputtering apparatus (see, e.g., Hamanaka, col. 12, ll. 10-12), forming silicide while sputtering metal and heating the substrate (see, e.g., Hamanaka, col. 12, ll. 12-26), removing the unreacted and partially oxidized metal (see, e.g., Hamanaka, col. 12, ll. 62-66), and performing an annealing process (see, e.g., Hamanaka, col. 12, ll. 66-67). Hamanaka discloses heating the semiconductor substrate, while depositing metal, at temperatures of 200°C (col. 12, ll. 13-15), 450°C (col. 8, ll. 43-48), or between 300°C and 400°C (col. 12, ll. 38-43). Hamanaka fails to disclose or suggest depositing a metal film while the semiconductor substrate is heated at a temperature of from greater than 450°C to 600°C.

Hamanaka fails to appreciate the potential time savings provided by the present invention. For example, after sputtering cobalt on the substrate while heating the substrate at a temperature from 200 degrees Celsius to 500 degrees Celsius, cobalt deposited on the N type gate electrode 205a, the P type gate electrode 205b, the N type source/drain region 209 and the P type source/drain region 210 chemically reacts with single crystalline silicon or polysilicon to form a dicobalt monosilicide (Co_2Si) film 212. Portions of the dicobalt monosilicide film 212a formed on the P type gate electrode 205b and the P type source/drain region 210 further chemically react with silicon to produce cobalt monosilicide (CoSi).

As discussed in the Declaration of Han attached hereto, experiments were performed on 24 substantially identical silicon wafers (i.e., one lot) to determine the processing time savings provided by the present invention, as compared to a conventional process reasonably close to the present invention ("Prior Art") and within the sputtering temperature range disclosed by Hamanaka (see paragraph 5 of the Declaration of Han, attached hereto). The "Prior Art" process sputtered cobalt at 200°C and subsequently formed silicide at 500°C, whereas the process representative of the present invention sputtered cobalt at 500°C. Except for the Co sputter deposition step and the existence (or lack of) cap metal sputter deposition and silicide formation steps, processing conditions for the "Prior Art" process and the present invention were substantially the same. In the "Prior Art" process, forming a TiN cap/barrier layer was necessary because the wafers had to be transferred to a Rapid Thermal Processing (RTP) chamber for silicide formation (see paragraph 6 of the Declaration of Han).

As shown in the table in paragraph 5 of the Declaration of Han, the present invention enables reducing the number of steps in the silicide formation process by 25% and the amount of time by 33%, both somewhat surprising results given the reasonable expectation that the invention would enable reduction of only one step in the conventional process (silicide formation; see paragraph 7 of the Declaration of Han), rather than two as observed. Another unexpected result from the present invention is that the present invention enables use of the RTP equipment for other processing (such as implant diffusion and activation) that would otherwise be used for silicide formation. This unexpected benefit is commercially very important when a

semiconductor wafer fabrication facility (commonly referred to as a "Fab") is capacity-constrained, because it enables other wafers to be processed more quickly as well (see paragraph 9 of the attached Declaration of Han).

In addition, two experiments were performed to form a metal silicide film, using the same processing equipment and the same recipe, except for the DC power (see paragraph 10 of the attached Declaration of Han). An Endura metal sputtering machine (from Applied Materials, Santa Clara, California) was used. Sputtering conditions included a wafer temperature of 200°C, using a cobalt (Co) metal target, a DC power of 2kW or 8kW (note that the deposition times were different at 2 kW vs. 8 kW to form a Co silicide film of substantially the same thickness), and a pressure of ~0.2 mTorr. A Ti thin film having a thickness of 480 Å was deposited on the metal silicide film. The substrate wafers (a bare Si wafer) was prepared identically, by cleaning with SC1 and HF, using conventional cleaning conditions. The results were as follows:

Sputtering Power	Silicide Resistance
2 kW	2.1 ohm/sq
8 kW	1.8 ohm/sq

Based on his experience in the field of semiconductor devices and manufacturing, it is Dr. Han's opinion that a manufacturing process that forms a metal silicide at less than 2 kW would likely not have a sufficiently low resistance to be commercially valuable. In other words, while such silicides could be expected to provide functional integrated circuits, such integrated circuits would be expected to have sufficiently high contact resistance (where the contact includes the metal silicide) to prevent the integrated circuit from exhibiting or achieving a commercially valuable signal processing speed (sometimes known as a "bin," which is frequently characterized by the length of time that a signal travels from input pin to output pin on the integrated circuit).

Hamanaka, however, is silent with regard to the sputtering power level. As a result, Hamanaka neither appreciates nor suggests the results provided by present invention. Therefore,

the rejection of claims 1, 2, 9, 12-14, 17, 18 and 21-23 in view of Hamanaka should be withdrawn.

The Rejection of Claims 3 and 4 under 35 U.S.C. § 103(a)

The rejection of Claims 3 and 4 under 35 U.S.C. § 103(a) as being unpatentable over Hamanaka in view of O'Brien (US 6,458,711) is respectfully traversed.

As explained above, Hamanaka is saliently deficient with regard to the results provided by the presently claimed invention. O'Brien fails to cure these deficiencies.

O'Brien relates to a method of forming silicide, including the steps of sputtering metal onto a substrate, and, in a separate step, inserting the coated substrate into a nitrogen atmosphere and raising the temperature to 600°C to create silicide (see, e.g., O'Brien, col. 2, ll. 54-62). O'Brien further discloses stripping residual metal (i.e., metal not used for the formation of silicide) with an SC1 solution (see, e.g., O'Brien, col. 3, ll. 40-55).

O'Brien forms silicide by heating the substrate to 600°C *after* sputtering metal onto the substrate. Furthermore, O'Brien is silent with regard to the sputtering power level. Therefore, O'Brien fails to cure the deficiencies of Hamanaka with respect to the present claims and the results provided thereby. Thus, no possible combination of Hamanaka and O'Brien can suggest or render obvious the present claims, and the rejection of Claims 3-4 under 35 U.S.C. § 103(a) as being unpatentable over Hamanaka in view of O'Brien should be withdrawn.

The Rejection of Claims 5-7, 10 and 19 under 35 U.S.C. § 103(a)

The rejection of Claims 5-7, 10 and 19 under 35 U.S.C. § 103(a) as being unpatentable over Hamanaka in view of Sumi (US 6,022,805) is respectfully traversed.

As explained above, Hamanaka is saliently deficient with regard to the results provided by the presently claimed invention. Sumi fails to cure these deficiencies.

Sumi relates to a method for removing native oxide on a silicide layer after the formation of the silicide (see, e.g., Sumi, col. 3, ll. 54-61). Sumi teaches that the silicide is formed by the conventional method of heating the substrate to 600°C *after* sputtering the metal (see, e.g., Sumi, col. 1, l. 65-col. 2, L 2). Furthermore, Sumi appears to be silent with regard to the DC sputtering power level (although various RF and microwave power levels are disclosed). Therefore, Sumi fails to cure the deficiencies of Hamanaka with respect to the present claims and the results provided thereby.

Thus, no possible combination of Hamanaka and Sumi can suggest or render obvious the present claims, and the rejection of Claims 5-7 under 35 U.S.C. § 103(a) as being unpatentable over Hamanaka in view of Sumi should be withdrawn.

The Rejection of Claims 11 and 20 under 35 U.S.C. § 103(a)

The rejection of Claims 11 and 20 under 35 U.S.C. § 103(a) as being unpatentable over Hamanaka in view of Wake (US 6,725,119) is respectfully traversed.

As explained above, Hamanaka is saliently deficient with regard to the results provided by the presently claimed invention. Wake fails to cure these deficiencies.

Wake relates to a process for designing a cleaning apparatus line configuration in a process for manufacturing a semiconductor device (see, e.g., Wake, col. 7, ll. 30-32), including an apparatus for cleaning semiconductors comprising silicide (see, e.g., Wake, col. 9, ll. 16-18). Wake teaches that the silicide is formed by the conventional method of heating the substrate to after sputtering the metal (see, e.g., Wake, Background, col. 3, ll. 25-30). Furthermore, Wake is silent with regard to the sputtering power level. Therefore, Wake fails to cure the deficiencies of Hamanaka with respect to the present claims and the results provided thereby.

Thus, no possible combination of Hamanaka and Wake can suggest or render obvious the present claims, and the rejection of Claims 5-7 under 35 U.S.C. § 103(a) as being unpatentable over Hamanaka in view of Wake should be withdrawn.

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Conclusions

In view of the above amendments and remarks, all bases for objection and rejection are overcome, and the application is in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,

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